TRENCH GROWTH TECHNIQUES USING SELECTIVE EPITAXY

BACKGROUND OF THE INVENTION

The present invention relates in general to trench semiconductor devices and, more particularly, to methods of forming trenches in a semiconductor devices.

Trench semiconductor devices are used in many applications including power supplies, battery chargers, computers, and cell phones. During the process used to manufacture trench semiconductor devices a dry silicon etch step is used to form the trenches in a silicon material of the semiconductor device. However, the channel region inside the trench wall of the semiconductor device is frequently damaged and rough edges can be formed after the dry silicon etch step. The damage to the channel region can cause leakage which then causes reduced carrier lifetime in the channel area. Decreased carrier lifetime increases the voltage threshold thereby increasing the on-state resistance of the semiconductor device. There is conventional prior art cleaning processes used to reduce the damage to the trench wall of the semiconductor device, but is at the cost of extra process steps. However, the extra process steps used to remove the damage to the trench walls frequently does not completely anneal the trench walls leaving the damage to the channel region in the semiconductor device.

Furthermore, the trench depth of a semiconductor device is typically a critical dimension which is difficult to meet using the dry silicon etch process.

For example, a trench power MOSFET device should have the trench depth just below the diffused body region to minimize the gate to drain capacitance and minimize the gate oxide electric field strength.

Accordingly, it is desirable to have a manufacturing process to form trenches in a semiconductor device without causing damage to the trench. Further, it is desirable to have the manufacturing process provide an accurate alignment of the trench bottom to specific dopant distribution during the process steps. The invention disclosed herein will address the above problems.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a cross-sectional view of a semiconductor device in a manufacturing step illustrating a masking step;

FIG. 2 is a cross-sectional view of the semiconductor device in the manufacturing step after an etching step;

FIG. 3 is a cross-sectional view of the semiconductor device in the manufacturing step illustrating a blanket epi growth technique;

FIG. 4 is a cross-sectional view of the semiconductor device in the manufacturing step illustrating a selective epi growth technique;

FIG. 5 is a cross-sectional view of a plurality of trenches in the semiconductor device; and

FIG. 6 is a cross-sectional view of a semiconductor device in the final stage of manufacturing using the process disclosed herein.

DETAILED DESCRIPTION OF THE DRAWINGS

FIG. 1 illustrates a cross-sectional view of a semiconductor device in a process step of a manufacturing process. FIG. 1 can be a metal oxide semiconductor field effect transistor (MOSFET) or an insulated gate bipolar transistor (IGBT). It will be apparent to someone skilled in the art that the process disclosed herein can be used to manufacture any one of these semiconductor devices. The method of making an n-channel MOSFET device is disclosed herein to illustrate the preferred process. However, the process can easily be used to make a p-channel MOSFET device.

A typical n-channel MOSFET semiconductor device shown in FIG. 1 includes foundation layer 12 grown on substrate 10. Foundation layer 12 is typically a lightly doped n-type silicon of typically $5x10^{16}$ atoms per cm^3 with dimensions in the range of five to fifty microns in thickness. Dimensions are determined for foundation layer 12 based on application. A thick layer ranging from twenty to thirty microns is typically used for foundation layer 12 for high voltage applications, where as a smaller thickness is used for low voltage applications. Substrate 10 is typically a highly doped n-type substrate of arsenic or phosphorous. A first layer, masking material 14, is grown on foundation layer 12. Masking material 14 is typically an oxide material, i.e. silicon dioxide, grown using a thermal oxide or can be deposited. A nitride material can also be used for masking material 14. Mask 16 is formed on masking material 14 where a trench is desired in the semiconductor device. Any typical photoresist material known to someone skilled in the art can be used for mask

16. An etch step is used to remove portions of masking material 14 where mask 16 is not formed leaving protruding portion 18 as shown in FIG. 2. Protruding portion 18 is a protruding portion of masking material 14 remaining after the etch step. Thus, protruding portion 18 will be made of a material of either silicon dioxide or nitride.

A dry etch process or any other similar process known to those skilled in the art is used in the etch step to remove portions of masking material 14. During this point in the process, an implant, implant 22, can be formed in foundation layer 12 at opening 20 shown in FIG. 2. Typically, implant 22 added at this point in the process is used for an IGBT device. An IGBT semiconductor device typically has a very low resistance, and as such turns off slowly. Adding implant 22 can modify and improve the turn-off of the IGBT semiconductor device. Implant 22 is formed in foundation layer 12. Implant 22 would typically be titanium or germanium. For an IGBT, foundation layer 12 would be a lightly doped n-type region.

A second layer, epi layer 24, is grown on foundation layer 12 adjacent to protruding portion 18 at opening 20 as shown in FIG. 3. Epi layer 24 is typically lightly doped p-type silicon of approximinatly $5x10^{17}$ atoms per cm^3. The growth of epi layer 24 is temperature controlled so that the layer only grows vertically above foundation layer 12 and not over protruding portion 18. For example, if foundation layer 12 is silicon and protruding portion 18 is oxide, the growth of epi layer 24 will only grow vertically where the silicon is exposed, and not where the oxide is exposed. Thus, epi layer 24 does not nucleate over the oxide material of protruding portion

18. The growth technique typically used to grow epi layer 24 is a selective epitaxial growth (SEG) process which is commonly known to someone skilled in the art. A cleaning polishing step is typically done after the SEG step to further smooth the surfaces of epi layer 24 and protruding portion 18.

An alternative to the SEG technique, is a blanket epitaxial growth (BEG) process which grows epi layer 24 as shown in FIG. 4. Epi layer 24 is grown over foundation layer 12 and protruding portion 18 using BEG. Epi layer 24 of FIG. 4 is polished back to ensure that protruding portion 18 is planarized with epi layer 24 as shown in FIG. 3. A polish step common to someone skilled in the art is chemical or mechanical polish (CMP). The BEG process grows an amorphous material such as a polysilicon material over protruding portion 18 and a crystalline material such as silicon over the exposed portions of foundation layer 12.

After the growth technique and polish step described above is completed, a non-damaging mask removal is used to remove protruding portion 18. Typically, the non-damaging mask removal technique is a wet oxide etch process. The wet oxide etch process is commonly known to someone skilled in the art as having a good selectivity between oxide and silicon material. Thus, the wet oxide etch process is used to remove protruding portion 18 to form trench 26 as shown in FIG. 5. The resulting trench 26 typically has squared corners at the junction to epi layer 24 and foundation layer 12. A silicon wet etch process is used to round off the corners at edge 28 of trench 26 shown in FIG. 5. Any other suitable wet etch process can be used to round off the corners as will be appreciated to someone skilled in the art. At this point

in the process implant 30 can be formed below trench 26 in foundation layer 12 as shown in FIG. 5. Implant 30 will typically be formed below trench 26 when making a MOSFET semiconductor device. The MOSFET semiconductor device has two parameters which can be modified using implants below the trench of the MOSFET. Namely, a lower device resistance, and an increase in the breakdown voltage. The device resistance can be reduced in a MOSFET semiconductor device by adding, for example, a phosphorous implant for implant 30. To raise the breakdown voltage of a MOSFET semiconductor device an implant of, for example, boron can be used for implant 30. The use of the above implants is typically known to someone skilled in the art, and is shown to illustrate the ease of using implants with the technique disclosed herein.

FIG. 6 illustrates a complete MOSFET semiconductor device formed using the above process. Once trench 26 is formed using the process, gate oxide layer 32 is disposed within trench 26. Gate oxide layer 32 is typically one to three hundered Angstroms in thickness. Gate structure 34 is disposed above gate oxide layer 32 within trench 26. Gate structure 34 is typically formed from a highly doped polysilicon with phosphorus of typically $2x10^{19}$ to $3x10^{19}$ atoms per cm^3. Source region 36 is typically a heavily doped n-type region formed within epi layer 24 adjacent to trench 26. Source region 36 is typically a shallow region of two tenths um in thickness. A typical dopant for source region 36 is an n-type arsenic doped region. Epi layer 24 further includes doped region 38 which is a heavily doped p-type region extending from the surface of epi layer 24. Doped region 38 typically has a higher doping

concentration than epi layer 24. Doped region 38 is typically formed to a depth of two to five tenths um and provides a low contact resistance between metal electrode layer 40 and epi layer 24. A typical dopant for doped region 38 is boron. ILD layer 42 is disposed on the top surface of epi layer 24 above gate structure 34 and source region 36. ILD layer 42 is typically silicon dioxide of approximately five thousand angtroms, and provides an isolation between metal electrode layer 40 and gate structure 34. Metal electrode layer 40 is formed above ILD layer 42 and on the top surface of epi layer 24 to provide a low resistive contact to source region 36 and doped region 38. Metal electrode layer 40 is typically an aluminum material.

It should be apparent to someone skilled in the art that the above process automatically aligns the depth of trench 26 to major surface 30 of foundation layer 12 as shown in FIG. 5. Prior art methods do not allow for an easy alignment of a trench and an epitaxial layer of a semiconductor device. The trench of a semiconductor device can be cut either too deep or too shallow. The process described herein provides a way to control the trench depth to avoid this problem. For example, in a power MOSFET device the optimum depth of a trench is at the interface between foundation layer 12 and masking material 14 as shown in FIG. 1. If the depth is too shallow the power MOSFET device will not work since no channel is formed, and if the depth is too deep, i.e. to far into foundation layer 12, the device will experience breakdown problems.

The following is an example in using the above described process. For example, it is desired to form a one micron deep trench for trench 26 using a five micron

thick foundation layer 12 to form the epitaxial layer of the semiconductor device. In the prior art, the dry etch process would be used to form the one micron deep trench in a five micron thick epitaxial layer by removing a one micron deep section of material from the five micron thick epitaxial layer. The prior art process produces two problems. First, the trench depth is difficult to control, and secondly, the resulting trench walls become damaged from the dry etch process. The process described herein mediates the above described problems in forming trench semiconductor devices. To form the same one micron deep trench, the process described herein starts with a four micron thick, for example, lightly doped n-type foundation layer 12. A one micron thick masking material 14, for example, silicon dioxide is grown on the four micron thick foundation layer 12. Mask 16 is formed on masking material 14 using photoresist at regions where a trench is desired as shown in FIG. 1. An etch step removes all of masking material 14 except at regions where mask 16 were formed. The etch step leaves a one micron thick protruding portion 18 as shown in FIG. 2. A dry etch process or any other type of process to those skilled in the art is used in the etch step. A one micron thick epi layer 24, using silicon for example, is grown on foundation layer 12 adjacent to protruding portion 18 at opening 20 as shown in FIG. 3. Epi layer 24 is grown using either the SEG or BEG process as described previously, and is typically well known to someone skilled in the art. The SEG process results in a one micron thick growth of silicon for epi layer 24. The BEG process requires a CMP to polish back epi layer 24 to planarize it with protruding portion 18 to form a one micron thick epi layer 24.

A wet oxide etch process is used to remove the one micron thick lightly doped n-type protruding portion 18, and leaving the one micron thick epi layer 24 of silicon. The wet oxide etch process is common to those skilled in the art. Thus, the etch process is not limited to the process described herein, and any other type of process can easily be used. The wet oxide etch process leaves a one micron deep trench 26 within the silicon of epi layer 24 as shown in FIG. 5. To complete the process, a silicon wet etch process is used to round off the corners shown in FIG. 5 at edge 28 of the one micron deep trench 26. The remaining process steps to complete the semiconductor device shown in FIG. 6 is known to someone skilled in the art.

Thus, the method of forming a trench in a semiconductor device described herein provides a process to form a trench without causing damage to the trench walls. The prior art processes typically cause trench wall damage by etching out the desired trench, where the process described herein builds the trench thereby eliminating trench wall damage. Further, the disclosed process provides accurate alignment of the trench bottom to specific dopant distributions formed in a semiconductor device.